WHAT IS CLAIMED IS:

1. A magnetic memory device comprising:

a plurality of first write lines;

a plurality of second write lines extending to intersect said plurality of first write lines respectively; and

a plurality of magnetoresistance elements each including a laminate including a magnetosensitive layer having a magnetization direction variable in accordance with an external magnetic field and adapted to allow an electric current to flow in a direction perpendicular to a laminated surface of said laminate, and an annular magnetic layer disposed on one surface side of said laminate so as to have an axial direction along said laminated surface and adapted to be penetrated by said first and second write lines;

wherein each memory cell is formed to include a pair of said magnetoresistance elements.

2. A magnetic memory device according to Claim 1, wherein said magnetosensitive layer and said annular magnetic layer are electrically connected.

3. A magnetic memory device according to Claim 1, wherein said magnetization directions of said magnetosensitive layers in said pair of magnetoresistance elements change to be antiparallel to each other due to magnetic fields generated by

electric currents flowing through said first and second write lines penetrating said annular magnetic layers respectively, so that information is stored in said memory cell in accordance with said first or second state.

4. A magnetic memory device according to Claim 3, wherein said memory cell is brought into one of a first state in which one of a pair of magnetosensitive layers in said pair of magnetoresistance elements is magnetized in a first direction while the other is magnetized in a second direction antiparallel to said first direction, and a second state in which one of said pair of magnetosensitive layers is magnetized in said second direction while the other is magnetized in said first direction, so that information is stored in said memory cell in accordance with said first or second state.

5. A magnetic memory device according to Claim 1, further comprising:

a pair of first read lines connected to said pair of magnetoresistance elements respectively and for supplying read currents to said magnetoresistance elements;

wherein information is read from said memory cell in accordance with an electric current flowing into each of said laminates.

6. A magnetic memory device according to Claim 5, wherein information is read from said memory cell in accordance with a difference between a pair of values of read currents supplied from said pair of read lines to said pair of magnetoresistance elements respectively.

7. A magnetic memory device according to Claim 6, further comprising:

a rectifying element provided on a current path of said read currents supplied to said pair of magnetoresistance elements; and

second read lines for introducing said read currents flowing through said pair of magnetoresistance elements to a ground.

8. A magnetic memory device according to Claim 7, wherein a pair of said rectifying elements are provided on current paths of said read currents supplied to said pair of magnetoresistance elements respectively.

9. A magnetic memory device according to Claim 8, wherein said pair of rectifying elements are provided between said pair of first read lines and said pair of magnetoresistance elements respectively.

10. A magnetic memory device according to Claim 8, wherein said pair of rectifying elements are provided between said pair of magnetoresistance elements and said pair of second read lines respectively.

11. A magnetic memory device according to Claim 7, wherein said rectifying elements are selected from Schottky diodes, PN junction diodes, bipolar transistors, and MOS (Metal-Oxide-Semiconductors) transistors.

12. A magnetic memory device according to Claim 6, further comprising:

a constant current circuit having a current regulating function for regulating a total sum of read currents flowing through a pair of magnetoresistance elements in each memory cell.

13. A magnetic memory device according to Claim 12, wherein said constant current circuit is arranged by use of a band gap reference.

14. A magnetic memory device according to Claim 12, wherein said constant current circuit is arranged by combination of a diode, a transistor and a resistor.

15. A magnetic memory device according to Claim 14,

wherein said transistor in said constant current circuit has not only said current regulating function but also a function as a first semiconductor switch for choosing whether to allow said read currents to flow into said pair of magnetoresistance elements or not.

16. A magnetic memory device according to Claim 12, wherein said constant current circuit is disposed between said second read lines and a ground.

17. A magnetic memory device according to Claim 6, further comprising:

a pair of current to voltage converting resistors provided between said pair of first read lines and a power supply respectively.

18. A magnetic memory device according to Claim 17, wherein each of said current to voltage converting resistors has a larger resistance value than a resistance value of each of said magnetoresistance elements.

19. A magnetic memory device according to Claim 17, further comprising:

a sense amplification circuit provided for each pair of said first read lines and for detecting and amplifying a

difference between read currents flowing in said first read lines as a voltage difference;

wherein terminals of said pair of current to voltage converting resistors on a side opposite to said power supply are connected to input terminals of said sense amplification circuit respectively.

20. A magnetic memory device according to Claim 19, further comprising:

a pair of second semiconductor switches provided on a side opposite to said power supply in said pair of current to voltage converting resistors and for choosing whether to supply said read currents to said pair of magnetoresistance elements or not, respectively;

wherein said pair of second semiconductor switches, said pair of current to voltage converting resistors and said sense amplification circuit are disposed integrally in one and the same area.

21. A magnetic memory device according to Claim 20, wherein said pair of second semiconductor switches, said pair of current to voltage converting resistors and said sense amplifier form symmetric circuits respectively.

22. A method for writing on a magnetic memory device

including: a plurality of first write lines; a plurality of second write lines extending to intersect said plurality of first write lines respectively; and a plurality of magnetoresistance elements each including a laminate including a magnetosensitive layer having a magnetization direction variable in accordance with an external magnetic field and adapted to allow an electric current to flow in a direction perpendicular to a laminated surface of said laminate, and an annular magnetic layer disposed on one surface side of said laminate so as to have an axial direction along said laminated surface and adapted to be penetrated by said first and second write lines; each memory cell being formed to include a pair of said magnetoresistance elements;

said method comprising the step of:

writing information into said memory cell by changing said magnetization directions of said magnetosensitive layers in said pair of magnetoresistance elements to be antiparallel to each other due to magnetic fields generated by electric currents flowing through said first and second write lines penetrating said annular magnetic layers.

23. A method for reading from a magnetic memory device including: a plurality of first write lines; a plurality of second write lines extending to intersect said plurality of first write lines respectively; and a plurality of magnetoresistance

elements each including a laminate including a magnetosensitive layer having a magnetization direction variable in accordance with an external magnetic field and adapted to allow an electric current to flow in a direction perpendicular to a laminated surface of said laminate, and an annular magnetic layer disposed on one surface side of said laminate so as to have an axial direction along said laminated surface and adapted to be penetrated by said first and second write lines; each memory cell being formed to include a pair of said magnetoresistance elements;

said method comprising the steps of:

supplying read currents to said pair of magnetoresistance elements in a direction perpendicular to laminated surfaces of laminates of said magnetoresistance elements respectively; and

reading information from said memory cell in accordance with said currents flowing through said laminates.

24. A method for reading from a magnetic memory device according to Claim 23, wherein information is read from said memory cell in accordance with a difference between a pair of values of read currents supplied to said pair of magnetoresistance elements respectively.

25. A magnetic memory device comprising:

a plurality of first write lines;

a plurality of second write lines extending to intersect said plurality of first write lines respectively;

a plurality of magnetoresistance elements each including a laminate including a magnetosensitive layer having a magnetization direction variable in accordance with an external magnetic field;

each memory cell being formed to include a pair of said magnetoresistance elements;

a pair of read lines for supplying read currents to said pair of magnetoresistance elements of said memory cell respectively;

a reading circuit for reading information from said memory cell in accordance with a difference between a pair of values of said read currents supplied to said pair of magnetoresistance elements through said pair of read lines respectively; and

a constant current circuit having a current regulating function for regulating a total sum of read currents flowing through a pair of magnetoresistance elements in each memory cell.

26. A magnetic memory device according to Claim 25, wherein said constant current circuit is arranged in combination of a diode, a transistor and a resistor, said transistor having not only said current regulating function but also a function as a semiconductor switch for choosing whether to allow said read currents to flow into said pair of magnetoresistance elements or not.